

## Universitas Negeri Surabaya Faculty of Engineering, Electrical Engineering Undergraduate Study Program

Document Code

## SEMESTER LEARNING PLAN

		CODE Course Family		C	Credit Weight			SEMESTER	Compilation Date	
CTOR & RONIC DEVICES		2020103303	Study Program Electronic Courses	ctive T	Г=0	P=0	ECTS=0	5	January 4, 2023	
ION		SP Developer		Course Cluster				Study Program Coordinator		
		L. Endah Cahya Ningrum, S	.Pd., M.Pd	Prof. Dr. I Suprianto	Baml b, M.1	bang F.		Dr. Lusia Rakhmawati, S.T., M.T.		
Project Based L	earning									
PLO study prog	gram w	hich is charged to the co	urse							
Program Objec	tives (I	PO)								
PO - 1	Studer	nts can explain about MOS tra	ansistors which consis	st of n-char	nnel	MOS	and p-cha	innel MOS types		
PO - 2	Studer the fou	nts are able to apply the digit indry.	al integrated circuit d	lesign stag	ges fr	om s	chematics	to designs read	ly to be sent to	
PO - 3	Studer	nts are able to explore CMOS	inverters as the most	t important	t circu	uit in o	digital circu	uit design.		
PO - 4	Students are able to explore CMOS inverters as the most important circuit in digital circuit design									
PO - 5	Studer	its are able to carry out analy	sis of the fabrication <b>p</b>	process.						
PO - 6	Students are able to carry out analysis on the realization of combinational circuits with static complementary CMOS and transmission gates.									
PO - 7	Students are able to carry out analysis of architectural design techniques for the radix-4 multiplier booth architecture.									
PO - 8	Studer	nts are able to explore analog	component design.							
PO - 9	Studer	ents are able to plan, design and evaluate sequential circuit simulations.								
PLO-PO Matrix	1									
PO Matrix at th	e end o	P.0         P0-1         P0-2         P0-3         P0-4         P0-5         P0-6         P0-7         P0-8         P0-9	ıb-PO)							
	Project Based L PLO Study prog Program Objec PO - 1 PO - 2 PO - 3 PO - 4 PO - 5 PO - 6 PO - 7 PO - 8 PO - 9 PLO-PO Matrix	TOR & RONIC DEVICES         ION         Project Based Learning         PLO study program w         Program Objectives (I         PO - 1       Studer         PO - 2       Studer         PO - 3       Studer         PO - 4       Studer         PO - 5       Studer         PO - 6       Studer         PO - 7       Studer         PO - 9       Studer	CODE         2020103303         ION       SP Developer         L. Endah Cahya Ningrum, S         Project Based Learning         PLO study program which is charged to the co         Program Objectives (PO)         PO - 1       Students can explain about MOS tra         PO - 2       Students are able to apply the digit the foundry.         PO - 3       Students are able to explore CMOS         PO - 4       Students are able to carry out analy         PO - 5       Students are able to carry out analy         PO - 6       Students are able to carry out analy         PO - 7       Students are able to explore CMOS         PO - 7       Students are able to carry out analy         PO - 8       Students are able to carry out analy         PO - 9       Students are able to plan, design ar         PLO-PO Matrix       PO-1         PO-2       PO-3         PO-4       PO-3         PO-5       PO-6         PO-6       PO-7         PO-8       PO-6         PO-7       PO-8         PO-6       PO-7         PO-8       PO-9         PO-9       PO-8         PO-9       PO-8         PO-9 <t< td=""><td>CODE         Course Family           27OR &amp; RONIC DEVICES         2020103303         Study Program Ele Courses           IDN         SP Developer           L. Endah Cahya Ningrum, S.Pd., M.Pd           Project Based Learning           PLO study program which is charged to the course           Program Objectives (PO)           P0 - 1         Students can explain about MOS transistors which consist Po - 2           Students are able to apply the digital integrated circuit of the foundry.           P0 - 3         Students are able to explore CMOS inverters as the mos PO - 4           Students are able to carry out analysis of the fabrication of the foundry.           P0 - 5         Students are able to carry out analysis of architectural de PO - 6           Students are able to carry out analysis of architectural de PO - 8           P0 - 9         Students are able to plan, design and evaluate sequentia PLO-PO Matrix           P0-4         PO-1           P0-5         PO-4           P0-6         PO-7           PO-8         PO-9           PO-7         PO-8           PO-7         PO-8           PO-6         PO-7           PO-8         PO-9           PO-7         PO-8           PO-7         PO-8           PO-7         &lt;</td><td>CODE         Course Family         Course family         Course family         Course family         Course family         Course family         Image: Course family         Course family         Image: Course family         <t< td=""><td>CODE         Course Family         Credit RoNiC DEVICES           2020103303         Study Program Elective Courses         T=0           ION         SP Developer         Course Clust Coordinator           IL         Endah Cahya Ningrum, S.Pd., M.Pd         Prof. Dr. Bamil Suprianto, M.T           Project Based Learning         Prof. Dr. Bamil Suprianto, M.T           Program Objectives (PO)         PO-1         Students can explain about MOS transistors which consist of n-channel Po-2           Po-1         Students are able to apply the digital integrated circuit design stages fi the foundy.         PO-3           PO-3         Students are able to explore CMOS inverters as the most important circu PO-4         Students are able to carry out analysis of the fabrication process.           PO-6         Students are able to carry out analysis of the realization of combinati and transmissing dates.         PO-6           PO-7         Students are able to carry out analysis of the realization of combinati and transmissing dates.         PO-7           PO-8         Students are able to carry out analysis of architectural design technique: PO-9         Students are able to plore analog component design.           PO-9         Students are able to plore, design and evaluate sequential circuit simulat PLO-PO Matrix         PO-6           PO-7         PO-8         PO-6           PO-7         PO-8         PO-7</td><td>CODE         Course Family         Credit Weil           TOR &amp; RONIC DEVICES         2020103303         Study Program Elective Courses         T=0         P=0           ION         SP Developer         Course Cluster Coordinator         Course Cluster Coordinator         For f. Dr. Barnbang Suprianto, M.T.           Project Based Learning         L. Endah Cahya Ningrum, S.Pd., M.Pd         Prof. Dr. Barnbang Suprianto, M.T.           Project Based Learning         PLO Study program which is charged to the course         Program Objectives (PO)           P0-1         Students are able to apply the digital integrated circuit design stages from s the foundry.         MOS           P0-3         Students are able to explore CMOS inverters as the most important circuit in in P0-4         Students are able to carry out analysis of the fabrication process.           P0-6         Students are able to carry out analysis of architectural design techniques for the and transmission gates.         Po-7           P0-7         Students are able to carry out analysis of architectural design techniques for the po-8         Students are able to plan, design and evaluate sequential circuit simulations.           P0-9         Students are able to plan design and evaluate sequential circuit simulations.         PO-1           P0-6         PO-1         PO-2         PO-3           P0-7         Students are able to plan, design and evaluate sequential circuit simulations.</td><td>CODE         Course Family         Credit Weight           TOR &amp; RONIC DEVICES         2020103303         Study Program Elective Courses         Te0         Pe0         ECTS=0           IDN         SP Developer         Course family         Prof. Dr. Bambang Suprianto, M.T.         Prof. Dr. Bambang           Project Based Learning         Program Objectives (PO)         Po1         Students can explain about MOS transistors which consist of n-channel MOS and p-cha           P0-1         Students are able to apply the digital integrated circuit design stages from schematics the foundly.         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Short Course Descript	tion	This course discuusing the project	isses semiconductor based learning metho	device d.	heory	and th	e bas	ic cor	ncepts	s of in	tegrat	ed circ	uit des	sign as	; well a	s how	to ana	lyze the
Referen	ces	Main :																
		1. S.M. Sze	.1985. Semiconducto	Devic	es Phys	sics an	id Tec	hnolc	ogy . J	ohn V	Viley &	& Sons						
		Supporters:																
		1. R.L. Geig 2. Neil H. W	jer, P.E. Allen, N.R. S ⁄aste, Kamran Eshrag	trader. ian. 19	1990. \ 39. Prin	LSI D	esign	I ech SL De	nique sign-	A Svs	nalog stem F	and Di	gital C ctive	ircuit . New Y	McGra ork: Ad	w-Hill Idisson.		
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Support lecturer	ting	3. Douglas Prof. Dr. Bamban L. Endah Cahya I	A. Pucknell, Kamran I g Suprianto, M.T. vingrum, S.Pd., M.Pd	Eshragi	an. 198	9. Bas		SI De	sign,	Syste	m and	l Circui	ts . Ne	w Delł	ni: Prer	itice Ha		
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Support lecturer Week- (1) 1	Fin. eac sta; (Su St ex tra co ch p-i ty	3. Douglas. Prof. Dr. Bamban L. Endah Cahya I al abilities of th learning ge b-PO) (2) udents can tplain about MOS ansistor which onsist of n- nannel MOS and channel MOS pes.	A. Pucknell, Kamran I g Suprianto, M.T. Vingrum, S.Pd., M.Pd Indicator (3) 1.Students can explain the characteristics of MOS transistors 2.Students can explain the MOS transistor 3.Students can explain the MOS transistor 1.Students can explain the MOS transistor 1.Attick the transistor 1.Attick the transistor	Eshragi raluatio Critit An pro gra the ba tru Part Test	n Criteria (( eria: alysis n cess o a answe sed on h). n of As cipator s	4 & Fo 4) 4) 4) 4) 4) 4) 4) 4) 4) 4) 4) 4) 4)	rm I (the g n ng to vided rel of <b>nent</b> :	Th let qu ar 10 as	Sign, Sign, Offlii offlii (5 rrougl ctures iestion Swers 00 mir ssignn	He Learn tuder [Es ne ( ne ) ) n s and s and nute nents	Ip Least In the second	arning nethoc ignme ed tim nline ( (	ls, Ne	e)	Lean mate Refer ( Materia Transis Sze.19	rning erials ences 7) al: MOS stor s and s and ology. /iley &	Ass Wr S S S	sessmer eight (% (8) 4%

OS h1.Students explain about MOS parasitic capacitance 2.Students explain about NMOS pass transistors 3.Students explain about PMOS pass transistors 4.Students explain about transmission gates 5.Students explain about multiple contactle tal to m1.Students are able to apply the CMOS process layer color system 3.Students are able to apply stick diagramsle S1.Students are able to apply the CMOS process layer color systemle s S1.Students are able to apply stick diagramsle S1.Students are able to carry ou analysis of CMOS circuits 2.Students are able to carry ou analysis of the static characteristics of CMOS inverters 3.Students	Students can explain about M transistors whic consist of n- channel MOS a p-channel MOS types. Students are ab to apply the dig integrated circui design stages fr schematic to design ready to sent to the found Students are ab to explore CMO inverters as the most important circuit design
Participatory Activitie         Tests         Criteria:         Analysis method (tr process of giving grades based on analysis according) the answers provide based on the level of truth).         Forms of Assessme : Participatory Activitie Project Results Assessment / Product Assessment, Tests         state         t	3.Students are able to apply stick diagrams       Tests         Students are able to explore CMOS inverters as the most important circuit in digital circuit design       1.Students are able to carry out analysis of CMOS circuits       Criteria: Analysis method (ft process of giving grades based on analysis of the static characteristics of CMOS inverters         3.Students are able to carry out analysis of the static       2.Students are able to carry out analysis of the static       Forms of Assessment         3.Students       explore CMOS inverters       3.Students       Participatory Activitie Project Results         4.Students       explore CMOS inverters       3.Students explore CMOS inverters       Students explore CMOS inverters         5.Students       explore Switching characteristics and interconnection effects on CMOS inverters       Students are able to carry out analysis about delays         6.Students are able to carry out analyses of power consumption       6.Students are able to carry out analyses of power consumption

6	Students are able to explore CMOS inverters as the most important circuit in digital circuit design	<ol> <li>Students are able to carry out analysis about inter-digitization</li> <li>Students are able to carry out an analysis of the width of the transistor</li> <li>Students are able to carry out analysis of metal interconnections</li> <li>Students are able to carry out analysis of inverter delay</li> <li>Students are able to carry out analysis of inverter delay</li> <li>Students are able to carpore inverter design and simulation</li> <li>Students are able to explore chain inverters</li> </ol>	Criteria: Analysis method (the process of giving grades based on analysis according to the answers provided based on the level of truth). Forms of Assessment : Participatory Activities, Project Results Assessment / Product Assessment, Tests	Using the discovery method with students carrying out knowledge exploration activities independently for 100 minutes	Material: CMOS Inverter Reference: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	3%
7	Students are able to carry out analysis of the fabrication process	<ol> <li>Students are able to carry out analysis of rule design</li> <li>Students are able to carry out analysis of design rules for transistors</li> </ol>	Criteria: Analysis method (the process of giving grades based on analysis according to the answers provided based on the level of truth). Forms of Assessment : Participatory Activities, Project Results Assessment / Product Assessment, Tests	Using the discovery method with students carrying out knowledge exploration activities independently for 100 minutes	Material: Fabrication process Reference: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	3%
8	UTS	Students can plan, complete and evaluate the results of the projects they have created	Criteria: 1. Explain accurately and clearly 2. Explain accurately and clearly; Presented comprehensively 3. Explain accurately and clearly; Delivered comprehensively; Based on analysis 4. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias 5. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias 5. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias; 5. Explained without bias; Information is conveyed with the support of facts Form of Assessment : Participatory Activities, Project Results Assessment / Product	By providing group project questions to be presented in class for 100 minutes	Material: MOS Transistor, Digital integrated circuit design stage, CMOS Inverter, Fabrication Process Library: SM Sze. 1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	20%
9	Students are able to carry out analysis on the realization of combinational circuits with static complementary CMOS and transmission gates.	<ol> <li>Students are able to carry out analysis of static complementary CMOS</li> <li>Students are able to carry out an analysis of transmission gates.</li> </ol>	Criteria: Analysis method (the process of giving grades based on analysis according to the answers provided based on the level of truth). Forms of Assessment : Participatory Activities, Project Results Assessment / Product Assessment, Tests	Using the discovery method with students carrying out knowledge exploration activities independently for 100 minutes	Material: Realization of combinational circuits Reference: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	3%

10	Students are able to carry out analysis of architectural design techniques for the radix-4 multiplier booth architecture	<ol> <li>Students are able to explore multiplier booths</li> <li>Students conduct an analysis of the performance of the multiplier booth</li> </ol>	Criteria: Analysis method (the process of giving grades based on analysis according to the answers provided based on the level of truth). Forms of Assessment : Participatory Activities, Project Results Assessment / Product Assessment, Tests	Using the discovery method with students carrying out knowledge exploration activities independently for 100 minutes	Material: Architecture of the radix-4 multiplier booth. <b>Reference:</b> <i>SM Sze.1985.</i> <i>Semiconductor</i> <i>Devices</i> <i>Physics and</i> <i>Technology.</i> <i>John Wiley &amp;</i> <i>Sons.</i>	3%
11	Students are able to explore analog component design.	<ol> <li>Students are able to carry out analysis of resistor design</li> <li>Students are able to carry out analysis of capacitor design</li> </ol>	Criteria: Analysis method (the process of giving grades based on analysis according to the answers provided based on the level of truth). Forms of Assessment : Participatory Activities, Project Results Assessment / Product Assessment, Tests	Using the discovery method with students carrying out knowledge exploration activities independently for 100 minutes	Material: Analog component design <b>Reference:</b> <i>SM Sze.</i> 1985. <i>Semiconductor</i> <i>Devices</i> <i>Physics and</i> <i>Technology.</i> <i>John Wiley &amp;</i> <i>Sons.</i>	3%
12	Students are able to plan, design and evaluate sequential circuit simulations	<ol> <li>Students can plan sequential circuits</li> <li>Students can complete sequential circuit designs</li> <li>Students can carry out evaluations on sequential series</li> </ol>	Criteria: Analysis method (the process of assigning values based on the results of the sequential circuit design). Form of Assessment : Participatory Activities, Project Results Assessment / Product Assessment	Using the inquiry method, students can solve problems through theoretical studies carried out in groups for 100 minutes	Material: Sequential Series Bibliography: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	5%
13	Students are able to plan, design and evaluate sequential circuit simulations	<ol> <li>Students can plan sequential circuits</li> <li>Students can complete sequential circuit designs</li> <li>Students can carry out evaluations on sequential series</li> </ol>	Criteria: Analysis method (the process of assigning values based on the results of the sequential circuit design). Form of Assessment : Participatory Activities, Project Results Assessment / Product Assessment	Using the inquiry method, students can solve problems through theoretical studies carried out in groups for 100 minutes	Material: Sequential Series Bibliography: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	5%
14	Students are able to plan, design and evaluate sequential circuit simulations	<ol> <li>Students can plan sequential circuits</li> <li>Students can complete sequential circuit designs</li> <li>Students can carry out evaluations on sequential series</li> </ol>	Criteria: Analysis method (the process of assigning values based on the results of the sequential circuit design). Form of Assessment : Participatory Activities, Project Results Assessment / Product Assessment	Using the inquiry method, students can solve problems through theoretical studies carried out in groups for 100 minutes	Material: Sequential Series Bibliography: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	5%
15	Students are able to plan, design and evaluate sequential circuit simulations	<ol> <li>Students can plan sequential circuits</li> <li>Students can complete sequential circuit designs</li> <li>Students can carry out evaluations on sequential series</li> </ol>	Criteria: Analysis method (the process of assigning values based on the results of the sequential circuit design). Form of Assessment : Participatory Activities, Project Results Assessment / Product Assessment	Using the inquiry method, students can solve problems through theoretical studies carried out in groups for 100 minutes	Material: Sequential Series Bibliography: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	4%

16	UAS	Students can plan, complete and evaluate the results of the projects they have created	Criteria: 1. Explain accurately and clearly 2. Explain accurately and clearly; Presented comprehensively 3. Explain accurately and clearly; Delivered comprehensively; Based on analysis 4. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias 5. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias 5. Explain accurately and clearly; Delivered comprehensively; Based on analysis; Explained without bias; Information is conveyed with the support of facts Form of Assessment : Project Results Assessment / Product Assessment	By providing group project questions to be presented in class for 100 minutes		Material: Realization of combinational circuits, Radix- 4 booth multiplier architecture, Sequential circuits Reference: SM Sze.1985. Semiconductor Devices Physics and Technology. John Wiley & Sons.	30%
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## Evaluation Percentage Recap: Project Based Learning

No	Evaluation	Percentage
1.	Participatory Activities	32%
2.	Project Results Assessment / Product Assessment	55.5%
3.	Test	12.5%
		100%

## Notes

- Learning Outcomes of Study Program Graduates (PLO Study Program) are the abilities possessed by each Study
  Program graduate which are the internalization of attitudes, mastery of knowledge and skills according to the level of their
  study program obtained through the learning process.
- 2. The PLO imposed on courses are several learning outcomes of study program graduates (CPL-Study Program) which are used for the formation/development of a course consisting of aspects of attitude, general skills, special skills and knowledge.
- Program Objectives (PO) are abilities that are specifically described from the PLO assigned to a course, and are specific to the study material or learning materials for that course.
- 4. **Subject Sub-PO (Sub-PO)** is a capability that is specifically described from the PO that can be measured or observed and is the final ability that is planned at each learning stage, and is specific to the learning material of the course.
- 5. Indicators for assessing abilities in the process and student learning outcomes are specific and measurable statements that identify the abilities or performance of student learning outcomes accompanied by evidence.
- Assessment Criteria are benchmarks used as a measure or measure of learning achievement in assessments based on predetermined indicators. Assessment criteria are guidelines for assessors so that assessments are consistent and unbiased. Criteria can be quantitative or qualitative.
- 7. Forms of assessment: test and non-test.
- 8. Forms of learning: Lecture, Response, Tutorial, Seminar or equivalent, Practicum, Studio Practice, Workshop Practice, Field Practice, Research, Community Service and/or other equivalent forms of learning.
- 9. Learning Methods: Small Group Discussion, Role-Play & Simulation, Discovery Learning, Self-Directed Learning,
- Cooperative Learning, Collaborative Learning, Contextual Learning, Project Based Learning, and other equivalent methods. 10. Learning materials are details or descriptions of study materials which can be presented in the form of several main points and sub-topics.
- 11. The assessment weight is the percentage of assessment of each sub-PO achievement whose size is proportional to the level of difficulty of achieving that sub-PO, and the total is 100%.
- 12. TM=Face to face, PT=Structured assignments, BM=Independent study.