	Universitas Negeri Surabaya **Faculty of Engineering** **, Electrical Engineering Education Undergraduate Study Program**	**Document Code**

SEMESTER LEARNING PLAN

Courses	CODE	Course Family	Credit Weight			SEMESTER	Compilation Date
Digital Electronics Practicum	8320102123	Compulsory Study Program Subjects	**T=2**	**P=0**	**ECTS=3.18**	3	July 17, 2024

AUTHORIZATION	SP Developer	Course Cluster Coordinator	Study Program Coordinator
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Learning model	**Project Based Learning**	
Program Learning Outcomes (PLO)	**PLO study program that is charged to the course**	
	PLO-5	Able to align the electrical and electronics engineering training curriculum in vocational education that is relevant to the demands of global industrial development (Education).
	PLO-7	Able to apply applied research to innovate vocational learning methods, optimize production process technology and electrical engineering services relevant to industry (Education).
	PLO-10	Have a responsible character and be committed to professional ethics (General/SSC4.6).
	Program Objectives (PO)	
	PO - 1	Students can describe, design and build basic prototypes of digital electronics consisting of: 7 Basic Logic Gates, Flip-flop, Counter Up. Counter Down, Encoder and Decoder, Shift Register, Multiplexer
	PLO-PO Matrix	

P.O	PLO-5	PLO-7	PLO-10
PO-1			

PO Matrix at the end of each learning stage (Sub-PO)

P.O	Week															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PO-1																

Short Course Description	Students can describe, design and create basic prototypes of digital electronics consisting of: 1. 7 Basic Logic Gates 2. Flip-flop 3. Counter Up 4. Counter Down 5. Encoder and Decoder 6. Shift Register 7. Multiplexer	
References	**Main :**	
	1. 1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, “Foundation Of Digital Electronic and Logic Design”. 2. 2. Daniel Adam Stek, “Analog and Digital Electronics”, 3rd edition.	
	Supporters:	
	1. 1. Palnitkar, Samit, “Verilog A guide to digital design”, 2nd Edition, Prentice Hall, 2003. 2. 2. Brown, Stephen, Vranesic, Zvonko, “Fundamental of digital logic with verilog design”, McGraw-Hill, 2003.	
Supporting lecturer	Dr. Meini Sondang Sumbawati, M.Pd. Miftahur Rohman, S.T., M.T. L. Endah Cahya Ningrum, S.Pd., M.Pd.	

Week-	Final abilities of each learning stage (Sub-PO)	Evaluation		Help Learning, Learning methods, Student Assignments, [Estimated time]		Learning materials [References]	Assessment Weight (%)
		Indicator	Criteria & Form	Offline (*offline*)	Online (*online*)		
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
1	Reviewing the theory of 7 Basic Logic Gates and Flip-flops	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** 7 Basic Logic Gates and Flip-flops **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	3%
2	Reviewing the theory of Counter Up and Counter Down	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Counter Up and Counter Down **Reference:** *2. Daniel Adam Stek, "Analog and Digital Electronics", 3rd edition.*	3%
3	Reviewing the theory of Encoders and Decoders, Shift Registers, and Multiplexers	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Encoder and Decoder, Shift Register, and Multiplexer **References:** *2. Brown, Stephen, Vranesic, Zvonko, "Fundamentals of digital logic with verilog design", McGraw-Hill, 2003.*	3%
4	Introduction to digital electronic circuit simulators (Proteus, Thinkercad, etc.)	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Introduction to digital electronic circuit simulators (Proteus, Thinkercad, etc.) **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	3%
5	Digital electronic circuit simulation: 7 Basic Logic Gates	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** 7 Basic Logic Gates and Flip-flops **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	3%

6	Digital electronic circuit simulation: Flip-flop	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Flip-flop **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	3%
7	Digital electronic circuit simulation: Counter Up	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Counter Up **Bibliography:** *2. Daniel Adam Stek, "Analog and Digital Electronics", 3rd edition.*	4%
8	UTS	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Practice/Performance, Test	Mid-term exam from the material and practicum that has been studied for 2x50 minutes		**Material:** **Library** Questions : *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	20%
9	Digital electronic circuit simulation: Counter Down	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Counter Down **Bibliography:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	4%
10	Digital electronic circuit simulation: Encoder and Decoder	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Encoders and Decoders **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	4%
11	Digital electronic circuit simulation: Shift Register and Multiplexer	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Shift Registers and Multiplexers **References:** *2. Daniel Adam Stek, "Analog and Digital Electronics", 3rd edition.*	4%
12	Practice 7 Basic Logic Gates and Flip-flops with project board	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** 7 Basic Logic Gates and Flip-flops with **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	4%

13	Practice Counter Up and Counter Down with the project board	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Counter Up and Counter Down **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	4%
14	Practice Encoder and Decoder, Shift Register, and Multiplexer with project board	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** Encoder and Decoder, Shift Register, and Multiplexer **References:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation of Digital Electronic and Logic Design".*	4%
15	Final practicum project: 7 Basic Logic Gates, Flip-flop, Counter Up. Counter Down, Encoder and Decoder, Shift Register, Multiplexer	Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Participatory Activities, Practice/Performance	Practical learning by giving lectures, questions and answers, and practicum for 2 x 50 minutes		**Material:** 7 Basic Logic Gates, Flip-flop, Counter Up. Counter Down, Encoder and Decoder, Shift Register, Multiplexer **Bibliography:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation Of Digital Electronic and Logic Design".*	4%
16		Evaluation Rubric	**Criteria:** Evaluation Rubric **Form of Assessment** : Test	Final Semester Exam from the material and practicum that has been studied		**Material:** 7 Basic Logic Gates, Flip-flop, Counter Up. Counter Down, Encoder and Decoder, Shift Register, Multiplexer **Bibliography:** *1. Sabir Kumar Sakar, Asish Kumar De, Souvik Sarkar, "Foundation Of Digital Electronic and Logic Design".*	30%

Evaluation Percentage Recap: Project Based Learning

No	Evaluation	Percentage
1.	Participatory Activities	25%
2.	Practice / Performance	35%
3.	Test	40%
		100%

Notes

1. **Learning Outcomes of Study Program Graduates (PLO - Study Program)** are the abilities possessed by each Study Program graduate which are the internalization of attitudes, mastery of knowledge and skills

according to the level of their study program obtained through the learning process.

2. **The PLO imposed on courses** are several learning outcomes of study program graduates (CPL-Study Program) which are used for the formation/development of a course consisting of aspects of attitude, general skills, special skills and knowledge.
3. **Program Objectives (PO)** are abilities that are specifically described from the PLO assigned to a course, and are specific to the study material or learning materials for that course.
4. **Subject Sub-PO (Sub-PO)** is a capability that is specifically described from the PO that can be measured or observed and is the final ability that is planned at each learning stage, and is specific to the learning material of the course.
5. **Indicators for assessing** ability in the process and student learning outcomes are specific and measurable statements that identify the ability or performance of student learning outcomes accompanied by evidence.
6. **Assessment Criteria** are benchmarks used as a measure or measure of learning achievement in assessments based on predetermined indicators. Assessment criteria are guidelines for assessors so that assessments are consistent and unbiased. Criteria can be quantitative or qualitative.
7. **Forms of assessment:** test and non-test.
8. **Forms of learning:** Lecture, Response, Tutorial, Seminar or equivalent, Practicum, Studio Practice, Workshop Practice, Field Practice, Research, Community Service and/or other equivalent forms of learning.
9. **Learning Methods:** Small Group Discussion, Role-Play & Simulation, Discovery Learning, Self-Directed Learning, Cooperative Learning, Collaborative Learning, Contextual Learning, Project Based Learning, and other equivalent methods.
10. **Learning materials** are details or descriptions of study materials which can be presented in the form of several main points and sub-topics.
11. **The assessment weight** is the percentage of assessment of each sub-PO achievement whose size is proportional to the level of difficulty of achieving that sub-PO, and the total is 100%.
12. TM=Face to face, PT=Structured assignments, BM=Independent study.